

Abstract of the Disclosure

A network processor that has multiple processing
5 elements, each supporting multiple simultaneous program
threads with access to shared resources in an interface.
Packet data is received from high-speed ports in segments and
each segment is assigned to one of the program threads. Each
packet may be assigned to a single program thread, two program
10 threads - one for header segment processing and the other for
handling payload segment(s) - or a different program thread
for segment of data in a packet. Dedicated inputs for ready
status and sequence numbers provide assistance needed for
receiving the packet data over a high speed port. The
15 dedicated inputs are used to monitor ready flags from the high
speed ports on a cycle-by-cycle basis. The sequence numbers
are used by the assigned threads to maintain ordering of
segments within a packet, as well as to order the writes of
the complete packets to transmit queues.

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